said providing information about processor activity includes providing information about substantially every instruction executed by the processor including instructions other than breakpoint instructions.

20. The method according to claim 19, wherein:

said providing information about processor activity includes providing an indication every time the processor stalls that the processor has stalled.

21. The method according to claim 19, wherein:

the information about processor activity includes an indication of at least one of whether the last instruction executed was a jump, a jump based on the contents of a register, a branch taken, or an instruction which encountered an exception.

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22. The method according to claim 19, further comprising:

c) providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump instruction based on the contents of a register.

23. The method according to claim 19, wherein:

said providing information is performed by the processor, and

said associating the instructions is performed by a debugger.

24. The method according to claim 19, wherein:

said step of providing information about processor activity in real time is performed according to a first clock; and

said step of associating the instructions executed by the processor with the information about processor activity is performed according to a second clock

25. A method of debugging a processor, said method comprising:

a) providing information about processor activity in real time according to a first clock; and

b) associating the instructions executed by the processor with the information about processor activity according to a second clock.

26. The method according to claim 25, wherein:

the first clock is the processor clock and the second clock is a debugger clock.

27. The method according to claim 25, wherein:

said providing information is performed by the processor, and

said associating the instructions is performed by a debugger.

28. The method according to claim 25, wherein:

said providing information about processor activity includes providing an indication every time the processor stalls that the processor has stalled.

29. The method according to claim 25, wherein:

the information about processor activity includes an indication of at least one of whether the last instruction executed was a jump, a jump based on the contents of a register, a branch taken, or an instruction which encountered an exception.

30. The method according to claim 25, further comprising:

c) providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump instruction based on the contents of a register.

31. A method of debugging a processor, said method comprising:

a) causing the processor to provide information about processor activity in real time; and

b) causing a debugger to associate the instructions executed by the processor with the information about processor activity.

32. The method according to claim 31, wherein:

said causing the processor to provide information about processor activity includes providing an indication every time the processor stalls that the processor has stalled.

33. The method according to claim 31, wherein:

the information about processor activity includes an indication of at least one of whether the last instruction executed was a jump, a jump based on the contents of a register, a branch taken, or an instruction which encountered an exception.

B/ cancelled 34. The method according to claim 31, further comprising:

c) providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump instruction based on the contents of a register.

35. The method according to claim 31, wherein:

said step of causing the processor to provide information about processor activity in real time is performed according to a first clock, and

said step of causing a debugger to associate the instructions executed by the processor with the information about processor activity is performed according to a second clock.